Listing of Claims

1. (Currently Amended) A noise ~~supression~~ suppression method, comprising:

generating a frequency signal from a PLL based on a reference signal; and

removing noise from the frequency signal by ~~shifting~~ setting a frequency divider in a feedback loop of the PLL to a value which shifts a spurious signal of a predetermined order outside a loop bandwidth of the PLL.

2. (Original) The method of claim 1, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter in the PLL.

3. (Original) The method of claim 1, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of a loop filter in the PLL.

4. (Original) The method of claim 1, wherein said noise is removed by:

shifting a first-order spurious signal outside the loop bandwidth of the PLL.

5. (Canceled)

6. (Original) The method of claim 5, wherein the frequency divider is set by a Sigma-Delta modulator.

7. (Original) The method of claim 6, wherein the frequency divider is a pulse swallow frequency divider.

8. (Original) The method of claim 7, further comprising:

computing a modulation ratio of the Sigma-Delta modulator based on the loop bandwidth of the PLL; and

setting the value of the pulse swallow frequency divider based on the modulation ratio computed for the Sigma-Delta modulator.

9. (Original) The method of claim 8, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

10. (Currently Amended) The method of claim 9, wherein the frequency signal of the PLL (f_{vco}) is generated in accordance with the following equation: $f_{vco} = \left(\frac{f_{ref}}{R}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$, where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

11. (Original) The method of claim 9, further comprising:

modulating the reference signal input into the PLL.

12. (Currently Amended) The method of claim 11, wherein the frequency signal of the PLL (f_{vco}) is generated in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{\text{mod}}}{D_{\text{mod}}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right),$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P ~~P~~$_{new}$ is the value of the program counter, S ~~S~~$_{new}$ is

the value of the swallow counter, $N_{\Sigma\Delta}$ ~~N_{new}~~ and $D_{\Sigma\Delta}$ ~~D_{new}~~ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

13. (Original) The method of claim 11, further comprising:

using the modulated reference signal as a comparison signal for the PLL as long as harmonics of the modulated reference signal and the unmodulated reference signal are not coincident.

14. (Original) The method of claim 1, wherein the spurious signal is generated by a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

15. (Currently Amended) A method for suppressing noise in a frequency generator, comprising:

modulating a reference signal; and

generating a frequency signal from a PLL based on the modulated reference signal, wherein modulating the reference frequency generates a frequency separation between harmonics of the modulated reference signal and the reference signal that suppresses noise in the frequency signal, wherein the modulated reference signal is used to generate the frequency

signal from the PLL as long as the harmonics of the modulated reference signal is not coincident with the harmonics of the reference signal.

16. (Canceled)

17. (Currently Amended) A frequency generator, comprising:

a phase-locked loop which generates a frequency signal based on a reference signal; and

a noise suppressor which shifts a spurious signal of a predetermined order outside a loop bandwidth of the PLL, wherein the noise suppressor includes:

a frequency divider in a feedback loop of the phase-locked loop; and

a controller which sets the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

18. (Original) The frequency generator of claim 17, wherein the phase-locked loop includes a loop filter, and the loop bandwidth is defined by a cutoff frequency of the loop filter.

19. (Original) The frequency generator of claim 17, wherein the phase-locked loop includes a loop filter, and the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of the loop filter.

20. (Original) The frequency generator of claim 17, wherein the noise suppressor shifts a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

21. (Canceled).

22 (Original) The frequency generator of claim 21, wherein the controller includes a Sigma-Delta modulator.

23. (Original) The frequency generator of claim 22, wherein the frequency divider is a pulse swallow frequency divider.

24. (Original) The frequency generator of claim 23, wherein the pulse swallow frequency divider is set to said value based on a modulation ratio of the Sigma-Delta modulator.

25. (Original) The frequency generator of claim 24, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

26. (Currently Amended) The method of claim 25, wherein the PLL generates the frequency signal (f_{vco}) in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right),$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

27. (Original) The frequency generator of claim 25, further comprising:

a modulator which modulates the reference signal input into the phase-locked loop.

28. (Currently Amended) The frequency generator of claim 27, wherein the PLL generates the frequency signal in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{\text{mod}}}{D_{\text{mod}}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right),$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P ~~P~~$_{new}$ is the value of the program counter, S ~~S~~$_{new}$ is the value of the swallow counter, $N_{\Sigma\Delta}$ ~~N~~$_{new}$ and $D_{\Sigma\Delta}$ ~~D~~$_{new}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

29. (Original) The frequency generator of claim 27, wherein the modulated reference signal is used as a comparison signal for the PLL as long as harmonics of the modulated reference signal are not coincident with harmonics of the unmodulated reference signal.

30. (Original) The frequency generator of claim 17, wherein the spurious signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

31. (Currently Amended) A frequency generator, comprising:

a modulator which modulates a reference signal; and

a PLL which generates a frequency signal based on the modulated reference signal, said modulator generating a frequency separation between harmonics of the modulated reference signal and the reference signal that suppresses noise in the frequency signal, wherein the PLL generates the frequency signal using the modulated reference signal as long as the

harmonics of the modulated reference signal are not coincident with the harmonics of the reference signal.

32. (Canceled).

33. (Currently Amended) A system for controlling a PLL, comprising:

a divider which divides a frequency signal output from the PLL; and

a controller which sets the divider to a value which shifts a spurious noise signal of a predetermined order outside the loop bandwidth of the PLL.

34. (Original) The system of claim 33, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter of the PLL.

35. (Original) The system of claim 33, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal and a cutoff frequency of a loop filter in the PLL.

36. (Original) The system of claim 33, the controller shifts a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

37. (Original) The system of claim 33, wherein the divider is a pulse swallow frequency divider and the controller includes a Sigma-Delta modulator.

38. (Original) The system of claim 37, wherein the Sigma-Delta modulator sets the value of the pulse swallow frequency divider based on a modulation ratio of the Sigma-Delta modulator.

39. (Original) The system of claim 38, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

40. (Currently Amended) The system of claim 39, wherein the controller controls the PLL

to generate the output frequency signal in accordance with the equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{\mathrm{mod}}}{D_{\mathrm{mod}}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right),$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

41. (Original) The system of claim 39, wherein the controller includes:

a modulator which modulates a reference signal of the PLL.

42. (Currently Amended) The system of claim 41, wherein the controller controls the PLL to generate the output frequency signal based on the equation

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{\text{mod}}}{D_{\text{mod}}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right),$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P ~~P~~$_{new}$ is the value of the program counter, S ~~S~~$_{new}$ is the value of the swallow counter, $N_{\Sigma\Delta}$ ~~N~~$_{new}$ and $D_{\Sigma\Delta}$ ~~D~~$_{new}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

43. (Original) The system of claim 41, wherein the modulated reference signal is used as a comparison signal of the PLL as long as a harmonic of the modulated reference signal is not coincident with a harmonic of unmodulated reference signal.

44. (Original) The system of claim 33, wherein the spurious noise signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

45. (New) The method of claim 1, wherein the spurious signal is generated from a mismatch in at least one of a charge pump and a phase/frequency detector in the PLL.

46. (New) The method of claim 45, wherein the mismatch in the charge pump includes a mismatch between UP and DOWN current sources.

47. (New) The method of claim 45, wherein the mismatch in the phase/frequency detector includes a mismatch between UP and DOWN signal paths in the phase/frequency detector.

48. (New) The method of claim 1, wherein the value of the frequency divider is set based on a modulation ratio of a Sigma-Delta modulator for removing the spurious signal.

49. (New) The method of claim 48,wherein the frequency divider is a pulse swallow frequency divider which includes a swallow counter and a program counter, and wherein values for at least one of the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator.

50. (New) The method of claim 48, wherein a numerator of the modulation ratio ($N_{\Sigma\Delta}$) is at least 50% of a denominator of the modulation ratio ($D_{\Sigma\Delta}$).

51. (New) The method of claim 50, further comprising:

modulating the reference signal into the PLL with a reference modulator, wherein the reference modulator has a modulation ratio (N_{mod}/D_{mod}) such that N_{mod} is at least 50% of D_{mod}.

52. (New) The method of claim 1, wherein setting the frequency divider includes:

adjusting at least one of a swallow counter and a program counter in the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

53. (New) The method of claim 1, further comprising:

shifting the reference signal to a fractional fixed value for input into a phase/frequency detector of the PLL, said fractional fixed value further shifing the spurious signal of said predetermined order.

54. (New) The frequency generator of claim 17, further comprising:

a frequency shifter which shifts the reference signal to a fractional fixed value for input into a phase/frequency detector of the PLL, said fractional fixed value further shifting the spurious signal of said predetermined order.

55. (New) The frequency generator of claim 31, wherein the modulator shifts the reference signal to a fractional fixed value that shifts the spurious signal of said predetermined order.